Information page

A:I/Os

INPUT:

//The following input are used for controlling oscillation frequency

1:ctrl1, input voltage range: 0/2.8V, input current: to transistor gate

2:ctrl2, input voltage range:0/2.8V , input current: to transistor gate

3:ctrl3, input voltage range:0/2.8V , input current: to transistor gate

4:ctrl4, input voltage range:0/2.8V , input current: to transistor gate

5:ctrl5, input voltage range:0/2.8V , input current: to transistor gate

//The following input are used for controlling oscillation amplitude

6:Vctrl, input voltage range: 0/2.8V, input current: to transistor gate

OUTPUT

//The following output are to the transmission line, each are 90 degree out of phase, the output //waveform is differential sine wave with a TBD commode voltage

1:Out0, output voltage range 1~2.8V, output current 36mA(TBD)

2:Out90, output voltage range 1~2.8V, output current 36mA(TBD)

3:Out180, output voltage range 1~2.8V, output current 36mA(TBD)

4:Out 270, output voltage range 1~2.8V, output current 36mA(TBD)

B: All Block layout size information:

1: Capacitance bank: amount 8, area 21um\*15um each

2: Core oscillator: amount 1, area 44um\*40um

3: Buffer: amount 1, area 60um\*80um (possible reduced to 60um\*60um)

4: Amp dec: amount 1, area 26um\*48um (possible reduce to 28um\*41um)

5: Vop dec: amount 1, area 26um\*48um (possible reduce to 28um\*41um)

6: Bias calc: amount 1, area 32um\*27um

7: Unknown buffer aunplifier , amount 1 estimate 24\*40um

C: number of channels: Require minimum of 3 channels and maximum of 9 channels. In the minimum case the channels are voltage measurement on Out0 and Vctrl, and the current measurement on Out0. In the maximum case, channels are voltage measurement onOut0, Out90, Out180, Out360, Vctrl, and the current measurement on Out0, Out90, Out180, Out360

D: The top 2 metals would not be occupied

E: The design needs a 2V power supply for PFET bias.